The STAR Scaler Board, A 10 MHz 24-bit VME Histogramming Module

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Abstract

This note describes a custom VME histogramming module, the STAR Scaler Board, developed for use in investigations of polarized proton interactions and high energy nucleus-nucleus collisions. It operates as a histogramming memory for which each of the 24 input bits corresponds to one bit of a 24 bit binary address in the memory array. On every tick of the input clock (RHIC strobe $\sim$ 10MHz) the contents of the memory location corresponding to the input address is incremented. Overflow occurs at 2^{40} or 10^{12} counts. The STAR experiment uses 12 Scaler boards to keep a continuous (deadtimeless) record of fast-detector and RHIC Accelerator-related correlations.

1 Introduction

One of the central problems in physics is to identify the origin of the spin carried by elementary particles. Experimental investigations typically employ polarized beams and targets in which specific quark- or gluon- moderated interactions are investigated to isolate the spin dependence. Such investigations are underway at the Relativistic Heavy Ion Collider (RHIC) at the Brookhaven National Laboratory (BNL) where colliding beams of polarized protons and of high energy nuclei are studied[1]. The scaler boards described here enable data collection for signals sensitive to polarization effects at the full 10 MHz rate.

RHIC typically runs with 120 bunches in each beam. The polarization of the protons is introduced by the source, the Alternating Gradient Synchrotron (AGS), with a typical polarization of $\geq 40\%$ spin up or spin down

in any given bunch. To better understand systematic effects in measuring spin dependent variables, some of the bunches are polarized with spin up, some with spin down, some are unpolarized and some are empty. Thus, at each interaction region, the pattern of the 120 bunches is complex, consisting of up-up, up-dn, up-none, dn-none, etc., each producing a different rate of quark-quark (qq), quark-gluon (qg), and gg interactions. The bunch patterns are stable for each fill of the collider, so that identifying the bunch numbers for each interaction allows the experiments to unfold the polarization content.

The Solenoidal Tracker at RHIC (STAR) experiment [2] is a nearly hermetic detector consisting of both very fast detectors, that respond for each beam crossing, and very slow detectors, that integrate for a time that covers many beam crossings. The fast detectors cover 2π in azimuthal angle ϕ and different regions of pseudo-rapidity ($\eta = -ln(tan(\theta/2))$, where θ is the polar angle). Because spin effects are often subtle it is necessary to compare large numbers of events for each of the polarization combinations. The scaler board described here was designed take data at a 10 MHz rate to correlate the fast detector data with the bunch number information to uncover the spin dependence of different signal combinations.

Data from the fast detectors consists of discriminator outputs from individual phototubes (PMT) as well as logic levels produced by the STAR Level 0 trigger electronics [3]. These signals can be aligned to the same bunch through appropriate digital delay logic on the scaler board where they are combined with a 7-bit binary pattern[1] that encodes the bunch number. For the polarization studies, the 24 input bits of the scaler board typically consist of 17 detector-related bits and 7 bunch-number bits. For unpolarized beam studies, the 24 input bits may consist of a mix of detector/logic bits and STAR status bits.

As a histogramming scaler, the module has 2^{24} memory locations and a word size of 40 bits at each location. The input clock at STAR is the RHIC bunch crossing clock ($\approx 10MHz$), called the RHIC Strobe (RS). The contents of the memory location addressed by the 24-bit input pattern present at each negative edge of the RHIC Strobe is incremented by 1. The 40 bit word size allows us to operate the board continuously for up to 24 hours without overflow, although in practice our integration times are typically less than 1 hour. The board can operate at lower input clock frequencies if longer integration times are required.

Two scaler boards can be operated as master/slave pairs allowing one to

[1] 7 bits encode up to 128 values

be read out while the other is accumulating data. The input signals are not terminated on the board to allow daisy-chain operation of the input signals. The input lines on each board are copied to an identical output connector. In typical ping-pong operation, the signals drop first in one unterminated board, are jumpered to another, and end in a board whose output lines are terminated (120Ω). Switching between the master/slave states is accomplished within a single clock cycle, with the master board controlling the operation and sending the switch order to the slave via a front panel LEMO connection. Many functions can be performed within the board under register control to eliminate or reduce time-consuming VME communication, such as clearing each memory cell or zero-suppressing output.

2 Technical description

The board consists of a central FPGA engine, two fast memories, front-panel input and VME backplane communication lines. In VME, the board occupies 0x10M (M= 1000000_{hex}) cells in memory space starting at its base address. This large memory space was chosen to facilitate VME DMA reading. The 128 megabytes of 32 bit memory is mapped for 8 bytes per channel, 3 bytes for address and 5 bytes for data. Operation is controlled by a series of 32 bit registers shown in Table 1 whose addresses (in bytes) begin at the board base address. Registers are named by their hex address, such that the register at address 4_{hex} is called *Reg4*. The contents of register 0 (*Reg0*) are fixed to return the pattern "deadf0c0" when read.

2.1 Input

The 24 bits of input and the input clock, hereafter called the RHIC strobe (RS), enter the board through a 50 pin DIN connector on the front panel. These signals are PECL pairs[2] on opposite pins. The RS signal enters on the first pair of pins, located at the bottom of the connector.

The board counts bits as one if their level is "high" on receipt of the negative edge of the RS pulse. Thus, if the input is a pulse it must be timed correctly. There are two modes of operation to facilitate pulse timing. These are set by *RegC* as either "classic" (bit=0) or "new" mode (bit=1) by a 24-bit mask. In "classic" mode, the input data is assumed to be pulses whose leading and trailing edges encompass the negative edge of the RS. In "new" mode, the scaler board sets a one shot on receipt of the input pulse leading

[2]Positive Emitter Coupled Logic

Register Name	Address$_{hex}$	read/write	Register Function
Board ID	0	r	HEX: deadf0c0
State	4	rw	scaler active
Memory Bank Select	8	rw	Memory bank Bit(0): (0=A, 1=B); Bit(1)=1: A+B (reading)
Input Mode Select	c	rw	bit=0→ classic mode (bitmask) bit=1→ new mode (bitmask)
Event Counter	10	rw	Least Significant 4 Bytes
Event Counter	14	rw	Most Significant 4 Bytes
Memory Clear Control	20	w	Bit(0)=1 initiates automated memory clear
Memory Clear Status	24	r	Bit(0)=1 indicates busy clearing memory
Zero Suppression Control	30	w	Bit(0)=1 starts the zero suppression Bit(1)=1 resumes the zero suppression
Zero Suppression Status	34	r	Bit(0)=1 indicates zero suppression done (no more non zero events)
Zero Suppression Busy	38	r	Bit(0)=1 indicates busy doing 0 suppression
Zero Suppression Size	3c	r	number of events in "0 suppression buffer"
Delay Registers	100-15c	rw	RHIC Strobe delay (100-input 0; 15c-input 23)
Vernier Delay Registers	200-25c	rw	12.5ns delay (200-input 0; 25c-input 23)
Pos Phase Offset Meter	300-35c	r	(300-input 0; 35c-input 23)
Neg Phase Offset Meter	400-45c	r	(400-input 0; 45c-input 23)
Zero Suppression Buffer	10000-11ffc	r	

Table 1: Register addresses

edge and clears this one shot 2.5 ns after the negative edge of the RS. This makes it easier to guarantee that an input signal is "high" when the RS negative edge occurs. A bit mask is used so that each of the 24 input bits can be treated as "classic" or "new" separately. For signals that persist in a state, such as those from the STAR Level0 electronics tree, the classic mode must be used.

The 24 input bits often arrive from different sources at different times, when in fact they represent an "event" and all should be considered "simultaneous". To align these bits in time the scaler board has two types of delays for each input bit, a 4-bit coarse and a 3-bit fine delay. The units of the coarse delay are RHIC strobe intervals ($\approx 100ns$), and the units of the fine delay are internal clock intervals. The internal clock is an 80 MHz oscillator

giving 12.5ns units. To determine the correct delays for each of the input signals, the board has phase-offset meters for each bit for both the leading (positive) and trailing (negative) edges (see Table 1). The values in registers 0x300 - 0x35C record the internal clock value relative to the RHIC strobe when the positive-going edge is detected, while registers 0x400-0x45C record the internal clock value when the negative-going edge is detected. Thus, to determine the correct delay setting for each signal, these registers can be read for a number of events and their mean value determined. This operation assumes that the relative bit timing is stable. Determining the coarse delay is accomplished by cycling through a set of coarse delays until the desired coincidence is achieved.

2.2 LEDs

There are 4 LEDs on the front of the board that are used to give visual indication of the board status. These are defined in Table 2.

LED(from top)	Function
1	Board active
2	Memory bank selected off→ Memory A; on→ Memory B
3	VME access in progress
4	not defined - blinking means board alive

Table 2: Front Panel LEDs

2.3 Operation

The boards contain 4 different types of jumpers to control operation as shown in Table 3. The 4 bits of address set by jumpers *A28-A31* allow up to 16 boards to share a crate, although this requires a particular kernal configuration for VME operation. The *A24* jumper determines whether a board is to be a "master" or a "slave". If a board is to be used in ping-pong between a "master" and a "slave" state, then jumper *J4* must be set appropriately. To allow RUN/STOP control via an external LEMO connection the *J6* jumper must be used.

The boards can be operated as "master"/"slave" pairs or as individuals (master without slave). Whether a board is active (counting) or off is controlled via *Reg4* as shown in Table 4. If the RUN/STOP jumper (*J6*) is on,

Jumper	Function
S1 A28-A31	Board base address
S1 A24	jumper in → Master: jumper out → Slave
J4	inter board communication OUT → Master : IN → Slave
J6	RUN STOP ON IN → Master : OUT → Slave

Table 3: Board jumper settings

Bit	Function
0	active master gated with RUN STOP ON
1	active slave (gated with RUN STOP ON
2	force active master
3	force active slave

Table 4: Scaler active register settings (*Reg4*))

then the board can be set to count only when the signal in the RUN/STOP LEMO (#2) is "high". With *J6* on, then the board can be set to count as a master when *Reg4=1* or as a slave when *Reg4=2*. Alternatively, if jumper *J6* is not on, then the board will "free run" as the "master" when *Reg4=4*, or as a "slave" when *Reg4=8*, ignoring the LEMO#2 input. When the register *Reg4* is set to 0, the board is not active and will not accumulate counts. The board must be set to inactive(*Reg4=0*) to be read. For test purposes, the user can write directly to the board when it is inactive, adressing each cell directly.

The board memories can be cleared using write commands as above, or the hardware clear option can be used. The hardware clear is much faster, since it does not require VME writes for each memory location. To use this option, the board is first made inactive (set *Reg4=0*) and then the hardware clear is initiated (set *Reg20=1*). The board will hold *Reg24=1* (high) until the memory is clear, and a software poll on this register can be used to wait until the memory clearing is complete.

In a ping-pong mode, the boards are set up to operate as a pair by connecting their LEMO#1 inputs together (see Table 5) and by setting the jumper *A24* (see Table 3) on one board to be the master and the other to be the slave. The master-board can then be made active using *Reg4*,

LEMO(from top)	Function
1(J5)	interconnection master/slave
2(J7)	"RUN-STOP" input on master

Table 5: Front panel LEMO connectors

setting it equal to 1 to run synchronously with an external signal in the "RUN/STOP" input, or setting it to 4 to free-run. The slave-board is left in the inactive state until the master is ready to be read out. Writing a 0 to the active register of the master causes the slave to begin operating on the next RS tick in the same mode that was set for the master, ie, gated with the external signal or free running. Since the master is now inactive, it is safe to begin the read cycle for the master.

2.4 Readout

The board uses 2 memory banks to meet the speed specification [3], so the sum for the channel is the sum of the two memories at that address. The two memory banks can be read separately (*Reg8=0 or 1*) or together (*Reg8=2*). For debugging, separate reading is desirable, while in operation, we use combined reads. The lower 32 bits of the count in each channel is at address "board base address + 0x8M + 8*channel" while the upper 8 bits are at "board base address + 0x8M + 8*channel + 4".

A count of the total number of clock cycles the board has integrated while in an active state is kept in *Reg10* (lower 4 bytes) and *Reg14* (upper 4 bytes). A check of the sum of all channel populations should equal this clock sum when running with the RUN/STOP requirement off.

Reading and writing each channel in the board using VME commands can be quite time consuming, although it is possible to do so for all data channels. For this reason the board has a zero suppression readout mode, initiated by setting *Reg30 = 1*. Note that *Reg38=1* when the board is busy doing the zero suppression. When being read with zero-suppression on, the FPGA looks at each channel, sums both memory banks for that channel, and copies those having non-0 counts into an intermediate buffer which holds 128 channels worth of information (1024 bytes). In this mode, the lower 4 bytes of the 5-byte sum are at "board base address + 0x10k + channel*8", with the upper byte at "board base address + 0x10k+channel*8+4". The

[3] with memory now available, (2005) we could duplicate the functionality with a single memory

channel number is held in the upper 3 bytes of the second read cycle. This buffer will be automatically replenished after each 128 channels are read until all non-zero channels are read. Set *Reg30=2* to process next 128 channels if required. When all non-zero channels have been read, the FPGA sets *Reg34=1*. The number of events in the zero-suppression buffer can be read from *Reg3C*.

3 Conclusion

The STAR experiment now has 12 of these scaler boards taking data at RHIC. They have been used successfully to measure transverse polarization components, to verify operation of the spin rotators, and to normalize all of the STAR data for Heavy Ion, for dAu, and for pp collisions.

References

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